

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Application No. 10/066,651
Attorney Docket No. Q64314

REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 31-36 have been added. Claims 3 and 18 have been cancelled. Claims 1, 4, 10, 13, 15, 17, 19 and 21 have also been amended. Claims 1, 2, 4-17 and 19-36 are now pending in the application, however, claims 23-27 have been withdrawn from consideration due to a restriction requirement.

In particular, claim 1 has been amended to also recite the features of dependent claim 3, claim 15 has been amended to also recite the features of dependent claim 18, and claim 17 has been rewritten in independent form to include all of the features of claim 15. The rejections are respectfully submitted to be obviated in view of the remarks presented herein.

As a preliminary matter, Applicant affirms the election made to Group 1 (claims 1-22 and 28-30), whereby claims 23-27 are withdrawn from further consideration by the Examiner. In addition, a Supplemental Application Data Sheet supplying the inventor's P.O. address is filed concurrently.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-14, 21, 22, 28 and 29 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1 and 10 have been editorially amended to define the variable "m" as an integer value, which are further defined in dependent claims as a unit that represents amount of data processing (e.g., a number of bits constituting a symbol, which may be appropriately determined according to a data representation

method, as recited in the specification on page 16, lines 1-5). This amount of data processing refers to the amount of data a single core of the decoder is able to process. Claims 13 and 21 have also been editorially amended to improve clarity. Accordingly, the rejection of claims 1-14, 21, 22, 28 and 29 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

Rejection Under 35 U.S.C. § 102(e) - Massoudi

Claims 1 and 10 have been rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Massoudi (U.S. Patent Number 6,363,511). The rejection is respectfully traversed.

Regarding amended independent claims 1 and 10, the claimed invention relates to a decoder comprising a storing part, a control part, a first RS core for calculating a first error location and a first error value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part.

Turning to the cited art, the disclosure of Massoudi does not anticipate the claimed invention. Massoudi describes a device for detecting and correcting errors in error correction coded data blocks read sequentially from a DVD medium. As shown in Figure 6, Massoudi's error detection and correction circuitry includes on-the-fly row correction circuitry 410, correction control circuitry 606, correction engine 608 and correction circuitry 602. However, Massoudi does not disclose a first RS core for calculating a first error location and a first error value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part, as claimed. Massoudi's correction engine 608 uses syndromes, generated by the on-the-fly row correction circuitry 410

and column and EDC syndrome generator circuitry 412, to “generate an ‘error value’ and ‘error location’ for the row or column associated with the syndrome” (column 9, lines 43-46). The generated error value is then used by either the on-the-fly row correction circuitry 410 or the correction circuitry 602 to correct the errors (column 9, lines 46-49). The on-the-fly row correction circuitry 410 and the correction circuitry 602 do not calculate error location/values. Instead, only Massoudi’s correction engine 608 calculates an error value and error location. On-the-fly correction circuitry 410 and correction circuitry 602 merely use the error location/values generated by the correction engine 608 (see column 9, lines 43-49). The claimed decoder comprises a first RS core as well as a second RS core, each calculating respective error location/values from data read from the storing part. At least by virtue of the aforementioned differences, the invention defined by claims 1 and 10 is patentable over Massoudi. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) are respectfully requested.

Rejection Under 35 U.S.C. § 102(e) - Fujita et al.

Claims 15 and 16 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Fujita et al. (U.S. Patent Number 6,131,178; hereinafter “Fujita”). The rejection is respectfully traversed.

Regarding amended independent claim 15, the claimed invention relates to a decoding method comprising reading data to be decoded and an eraser flag, calculating an error location and an error value from the read data, correcting an error of the data according to the calculated error location and error value, and decoding the data. The calculation step comprises a first

calculation step for calculating a first error location and a first error value from the read data, and
a second calculation step for calculating a second error location and a second error value from
the read data.

Turning to the cited art, the disclosure of Fujita does not anticipate the claimed invention. Fujita describes an error correction apparatus for singly extended Reed-Solomon code or double extended Reed-Solomon code. The Examiner cites to Figures 21 and 24 as teaching the claimed invention, however, there is no showing or mention in Fujita of both a first calculation step for calculating a first error location and a first error value from the read data, and a second calculation step for calculating a second error location and a second error value from the read data. Furthermore, the Examiner admits in paragraph 7 of the Office Action that “Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders].” At least by virtue of the aforementioned differences, the invention defined by claim 15 is patentable over Fujita. Claim 16 is a dependent claim including all of the limitations of independent claim 15, which, as established above, is patentable over Fujita. Therefore, claim 16 is patentable over Fujita for at least the aforementioned reasons as well as for its additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) are respectfully requested.

With further regard to claim 16, the data is read in (2m) bit units in the data reading step. Fujita does not at all mention data to be decoded being read in (2m) bit units. At least by virtue of these additional differences, the invention defined by claim 16 is patentable over Fujita.

Rejection Under 35 U.S.C. § 103(a) - Massoudi in view of Fujita et al.

Claims 4-9, 11-14, 28 and 29 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Massoudi in view of Fujita. The rejection is respectfully traversed.

Referring to amended independent claims 1 and 10, the claimed decoder comprises a first RS core as well as a second RS core, each calculating respective error location/values from data read from the storing part. Neither Massoudi nor Fujita disclose both a first RS core for calculating a first error location and a first error value from data read from the storing part, and a second RS core for calculating a second error location and a second error value from data read from the storing part, as claimed. Instead, only Massoudi's correction engine 608 "generate[s] an 'error value' and 'error location' for the row or column associated with the syndrome" (column 9, lines 43-46). On-the-fly correction circuitry 410 and correction circuitry 602 solely use the error location/values generated by the correction engine 608 (see column 9, lines 43-49), and do not themselves generate any error value or error location.

Turning to Fujita, the Examiner further admits in paragraph 7 of the Office Action that "Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders]." Thus, Fujita also does not disclose both a first RS core and a second RS core, as claimed. At least by virtue of the aforementioned differences, the invention defined by independent claims 1 and 10 is patentable over Massoudi in view of Fujita. Claims {4-9} and {11-14, 28 and 29} are dependent claims including all of the limitations of independent claims 1 and 10, respectively, which, as established above, is patentable over Massoudi in view of Fujita. Therefore, claims 4-9, 11-14, 28 and 29 are patentable over Massoudi in view of Fujita for at least the aforementioned reasons

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as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Rejection Under 35 U.S.C. § 103(a) - Fujita et al. in view of Massoudi

Claims 19-22 and 30 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fujita in view of Massoudi. The rejection is respectfully traversed.

Regarding amended independent claim 15, the claimed decoder comprises both a first calculation step for calculating a first error location and a first error value from the read data, and a second calculation step for calculating a second error location and a second error value from the read data. The Examiner admits in paragraph 7 of the Office Action that “Fujita does not explicitly teach the specific use of two Reed-Solomon [decoders].” Massoudi also does not disclose both a first calculation step and a second calculation step, as claimed. As described above, Massoudi does not use two Reed-Solomon decoders, as Examiner contends. Instead, it is only Massoudi’s correction engine 608 that “generate[s] an ‘error value’ and ‘error location’ for the row or column associated with the syndrome” (column 9, lines 43-46). On-the-fly correction circuitry 410 and correction circuitry 602 solely use the error location/values generated by the correction engine 608 (see column 9, lines 43-49), and do not themselves generate any error value or error location. Thus, Massoudi only teaches a single calculation step/core. At least by virtue of the aforementioned differences, the invention defined by independent claim 15 is patentable over Fujita in view of Massoudi. Claims 19-22 and 30 are dependent claims including all of the limitations of independent claim 15, which, as established above, is patentable over Fujita in view of Massoudi. Therefore, claims 19-22 and 30 are patentable over Fujita in view of

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Massoudi for at least the aforementioned reasons as well as for their additionally recited features.

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) are respectfully requested.

Newly Added Claims

Claims 31-36 are newly added by this Amendment and are believed to be in condition for allowance.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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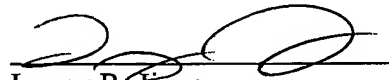
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